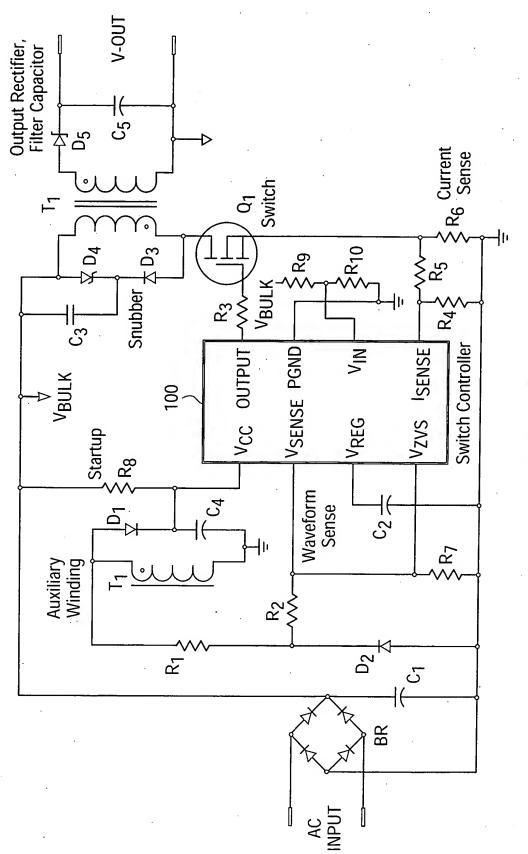


REPLACEMENT SHEET

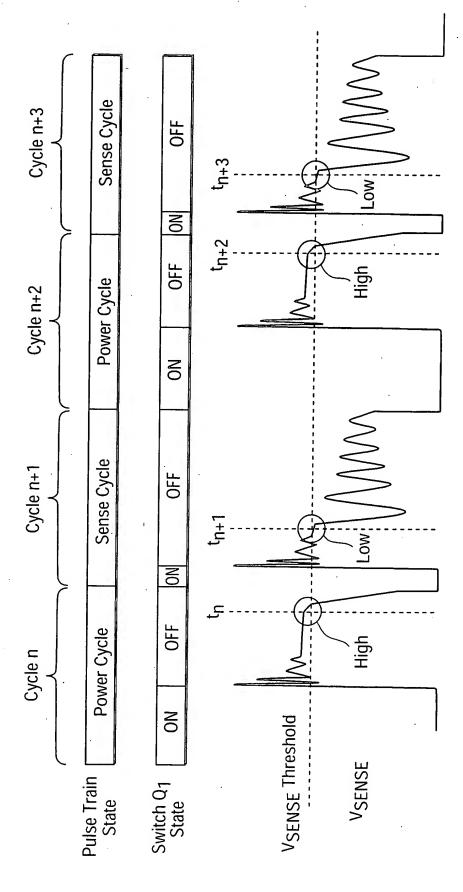
Title: Power Converter Controller Having Event
Generator for Detection of Events and
Generation of Digital Error
Inventors: Mark D. Eason, et al.
Application No.: 10/735,211
Sheet 1 of 10



REPLACEMENT SHEET

Title: Power Converter Controller Having Event Generator for Detection of Events and

Generation of Digital Error Inventors: Mark D. Eason, et al. Application No.: 10/735,211 Sheet 2 of 10



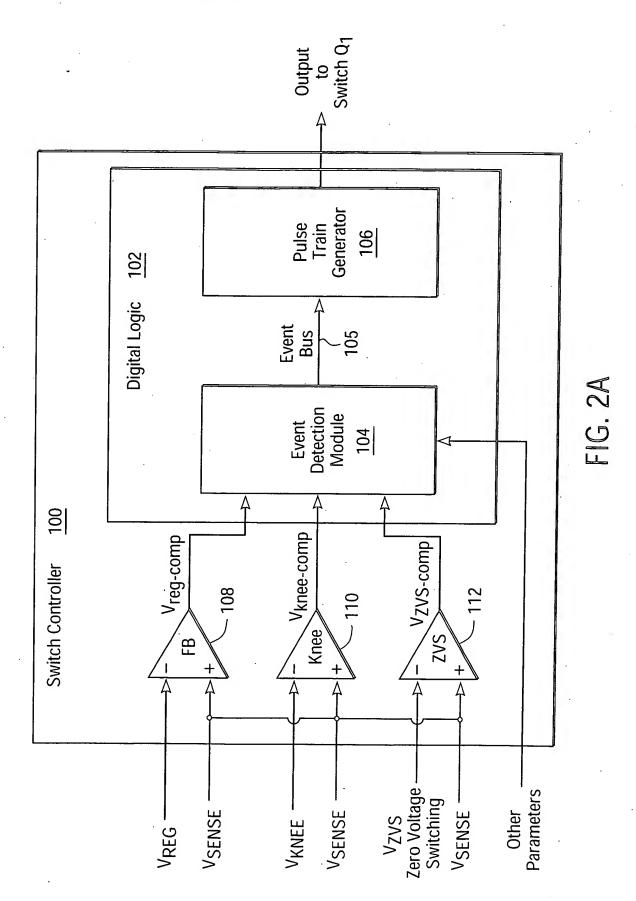
VSENSE is measured at a point near the end of the OFF period. This voltage is compared to the VSENSE threshold. If it is higher, the next cycle is a sense cycle. Otherwise, the next cycle is a power cycle.

REPLACEMENT SHEET

Title: Power Converter Controller Having Event
Generator for Detection of Events and
Generation of Digital Error

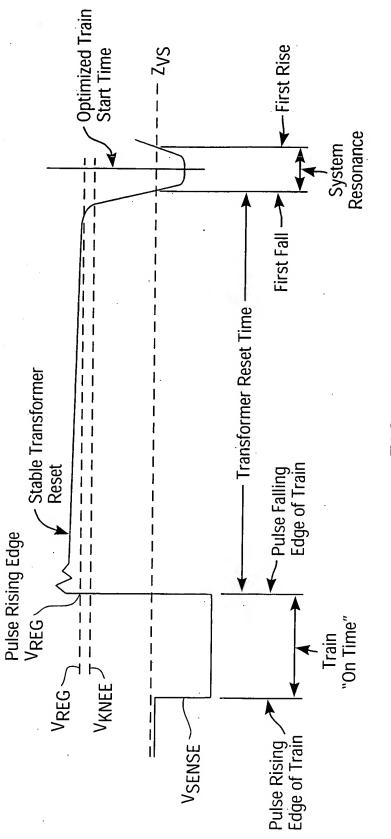
Inventors: Mark D. Eason, et al.
Application No.: 10/735,211

Sheet 3 of 10

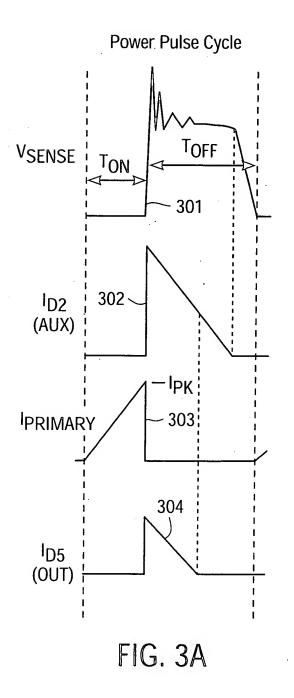


REPLACEMENT SHEET
Title: Power Converter Controller Having Event

Generator for Detection of Events and Generation of Digital Error Inventors: Mark D. Eason, et al. Application No.: 10/735,211 Sheet 4 of 10



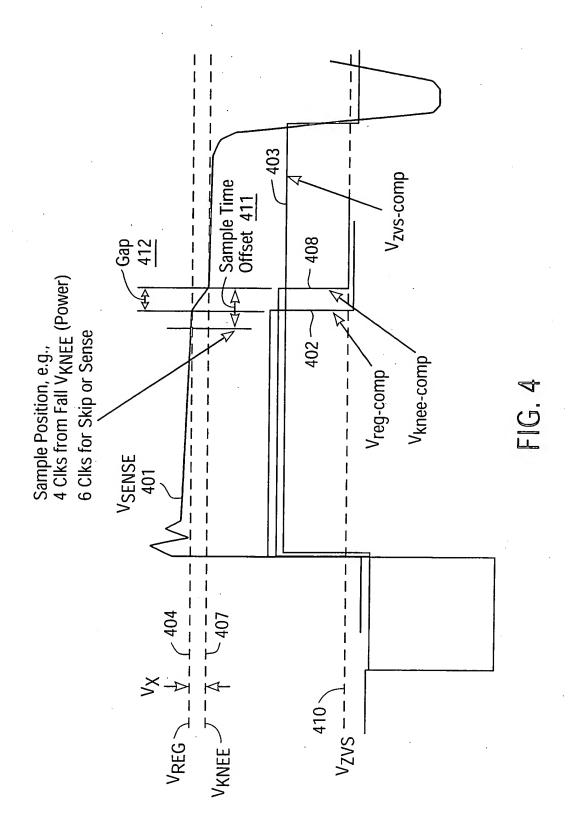
Generation of Digital Error Inventors: Mark D. Eason, et al. Application No.: 10/735,211 Sheet 5 of 10



Power Pulse Cycle -305 TOFF TON V_{SENSE} I_{D2} (AUX) 306 **IPK IPRIMARY** - 307 I_{D5} (OUT) 308 FIG. 3B

REPLACEMENT SHEET

Title: Power Converter Controller Having Event
Generator for Detection of Events and
Generation of Digital Error
Inventors: Mark D. Eason, et al.
Application No.: 10/735,211
Sheet 6 of 10



REPLACEMENT SHEET

Title: Power Converter Controller Having Event
Generator for Detection of Events and
Generation of Digital Error
Inventors: Mark D. Eason, et al.
Application No.: 10/735,211
Sheet 7 of 10

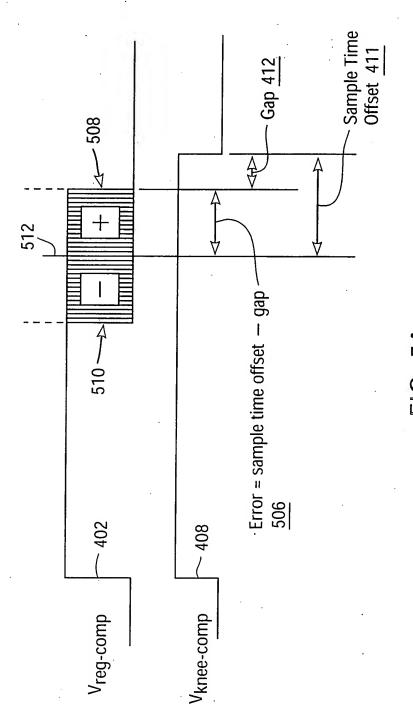
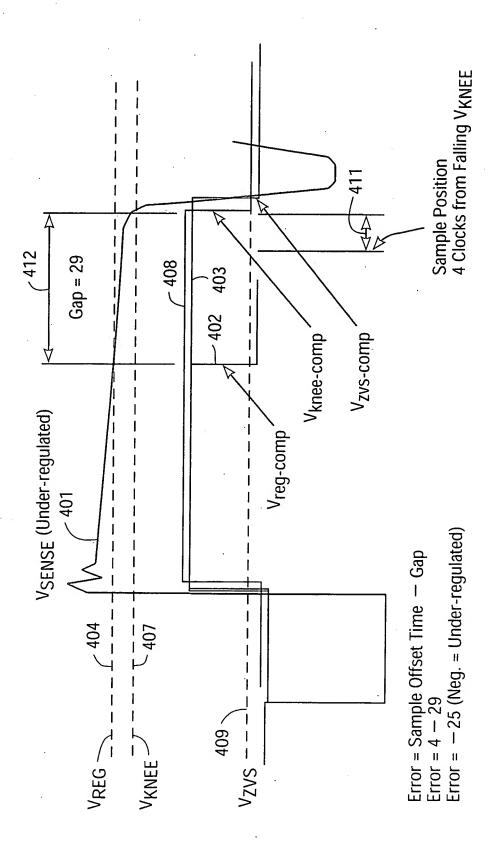
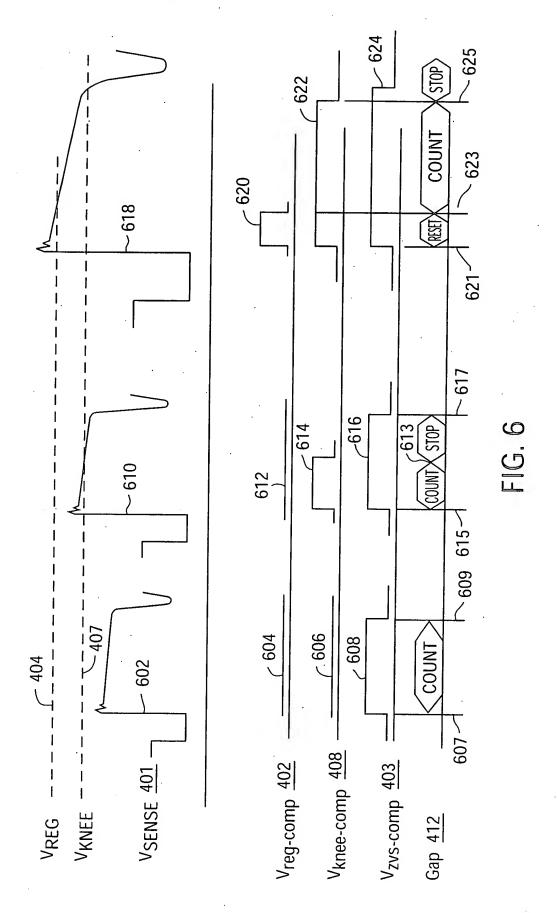


FIG. 5A

Generation of Digital Error Inventors: Mark D. Eason, et al. Application No.: 10/735,211 Sheet 8 of 10



Generation of Digital Error Inventors: Mark D. Eason, et al. Application No.: 10/735,211 Sheet 9 of 10



Generation of Digital Error Inventors: Mark D. Eason, et al. Atty. Docket No.: 23516-07980 Sheet 10 of 10

